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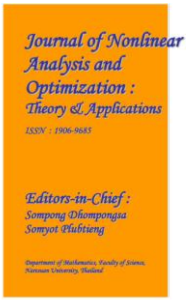
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Sompong Dhompongsa
Somyot Plubtieng
Department of Mathematics, Faculty of Science, Naresuan University, Thailand

Low Power 4:1 Mux Design Using Voltage Scaling Technique

Mr .S .Ahmed Basha [1],D. Ahemed Aswaq [2], P.Sreekanth [3], G. Vinay Kumar [4],B. Hari Krishna [5], B. Dinesh [6]

[1]Assistant Professor, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India [2]Student, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India [3]Student, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India [4]Student, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India [5]Student, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India [5]Student, ECE Dept., St.Johns College of Engg. & Tech., Yemmiganur, Kurnool(Dist.), 518360, India

Abstract: Minimizing power consumption is critical in digital electronics, especially for portable, battery-operated devices. This paper presents a low power 4:1 multiplexer (MUX) design using voltage scaling, a technique that reduces dynamic power dissipation by lowering the supply voltage. The goal is to achieve significant power reduction while maintaining acceptable performance levels. The methodology includes CMOS-based schematic design, voltage scaling application, and subsequent simulation and optimization using advanced Electronic Design Automation (EDA) tools. Results show that the voltage-scaled MUX significantly reduces power consumption compared to conventional designs. Key performance metrics such as power consumption, propagation delay, and power-delay product (PDP) are analyzed to balance power efficiency and performance. Voltage scaling effectively enhances power efficiency in digital circuits, particularly in multiplexers, but increases propagation delay, requiring careful optimization. This research provides a framework for low power digital designs, offering insights and guidelines for future advancements in power-efficient electronics. The results suggest promising applications for voltage scaling in various digital components.

Keywords: Low Power, 4:1 Multiplexer, Voltage Scaling, CMOS, Power Consumption, Digital Circuits.

I. INTRODUCTION-4:1 MUX:

It quite often happens, in the design of large-scale digital systems, that a single line is required to carry two or more different digital signals. Of course, only one signal at a time can be placed on the one line. What is required is a device that will allow us to select, at different instants, the signal we wish to place on this common line. Such a circuit is referred to as Multiplexer. The graphical symbol and truth table of 4:1 MUX are shown in Fig. 1.and Fig. 2 respectively. A multiplexer performs the function of selecting the input on any one of ‘n’ input lines and feeding this input to one output line.

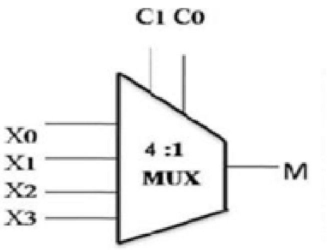
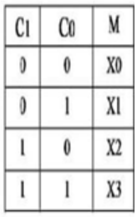


Fig:1 :- 4:1 MUX



C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

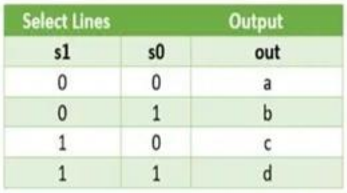
Fig:2:- Truth table

Multiplexers are used as one method of reducing the number of integrated circuit packages required by a particular circuit design. This in turn reduces the cost of the system.

I .a.Gate level modeling:

The gate-level abstraction is the lowest level of modeling. The switch level model is also a low level of modeling but it isn’t that common. The gate-level modeling style uses the built-in basic logic gates predefined in Verilog. We only need to know the logic diagram of the system since the only requirement is to know the layout of the particular logic gates.

Truth table:



Select Lines		Output
s1	s0	out
0	0	a
0	1	b
1	0	c
1	1	d

TABLE:1. Truth table

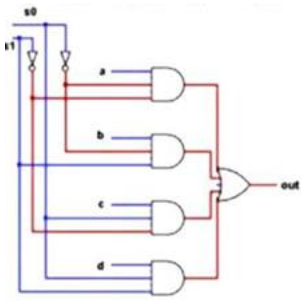


Fig 3 Logic Diagram of 4 : 1 MUX Now, this circuit shows we need two NOT gates, four AND gates, and one OR gate for implementing the 4×1 MUX in gate- level modeling.

I POWER DISSIPATION

I.a. Sources of power dissipation

Power is the instantaneous power in the device, while energy is the integration of power with time. 4 illustrates the difference between power energy. For example, in Fig. 4 we can see that approach 1 takes less time but consumes more power than approach 2. But the energy consumed by the two, that is, the area under the curve for both the approaches is the same, and the battery life is primarily determined by this energy consumed.

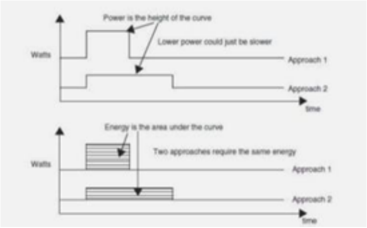


Fig.4:Power versus Energy

Types of Power Dissipations

❖Dynamic power is the power consumed when the device is active, that is, when the signals of the design are changing values.

❖Static power is the power consumed when the device is powered up but no signals are changing value. In CMOS devices, the static power consumption is due to leakage mechanism. Various components of power dissipation in CMOS devices can therefore be categorized as shown in Fig 5

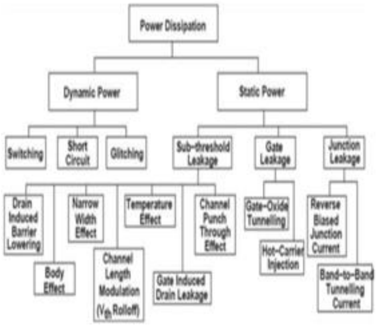

Power Dissipation
Dynamic Power
Static Power
Switching
Short Circuit
Glitching
Sub-threshold Leakage
Gate Leakage
Junction Leakage
Drain Induced Barrier Lowering
Body Effect
Narrow Width Effect
Channel Length Modulation (V_{th} Rolloff)
Temperature Effect
Gate Induced Drain Leakage
Channel Punch Through Effect
Gate-Oxide Tunnelling
Hot-Carrier Injection
Reverse Biased Junction Current
Band-to-Band Tunnelling Current

Fig.: 5 Types of power dissipation

Static Power

Static power is the power consumed when there is no circuit activity or you can say, when the circuit is in quiescent mode. In the presence of a supply voltage, even if we withdraw the clocks and don’t change the inputs to the circuit, the circuit will still consume some power, called the static power consumption.

It is mainly due to the leakage currents that flows, when the transistor is in off-state. There are many types of leakage currents, however in the diagram below I have shown only two common leakage currents.

Reverse bias leakage current flows when the junction diodes within the transistors are reverse biased. Similarly sub- threshold leakage current flows from drain to source through the channel, when VGS ≲ Vth [Vth is the threshold voltage of the transistor]. Typically the leakage power dissipation in a transistor is inversely proportional to its threshold voltage.

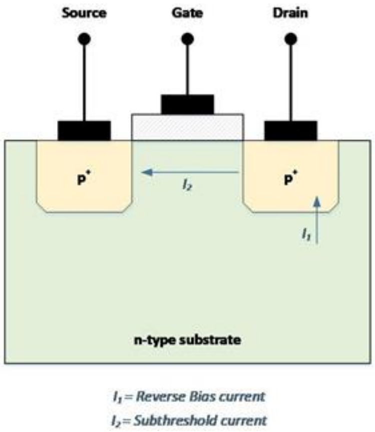

Source
Gate
Drain
p^+
I_2
p^+
I_1
n-type substrate
I_1 = Reverse Bias current
I_2 = Subthreshold current

Fig. 6 : Leakage currents in a PMOS transistor

Dynamic Power

Dynamic power is the power consumed when the circuit is in operation, which means we have applied supply voltage, applied clock and changing the inputs.

It is mainly due to the dynamic currents, such as capacitance currents (switching power) and short-circuit currents (short-circuit power).

III. Implementation and Result

III.a.80nm Layout Diagrams and Simulation:

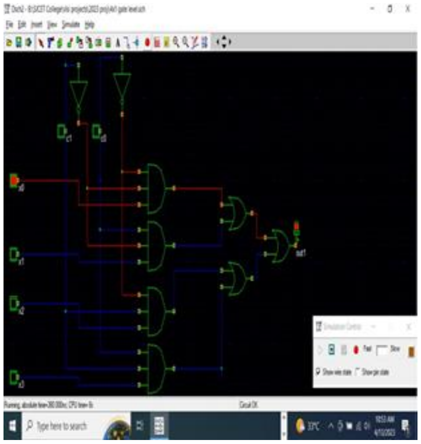


Fig. 7: Schematic diagram of gate level 4:1mux.

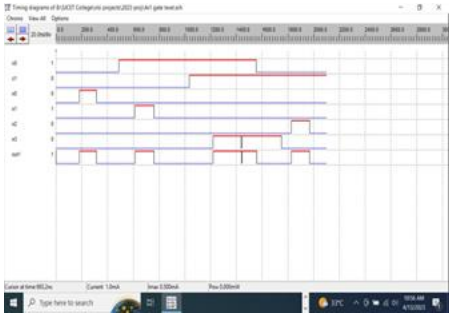


Fig. 8 : Timing diagram of Gate Level 4:1 Mux

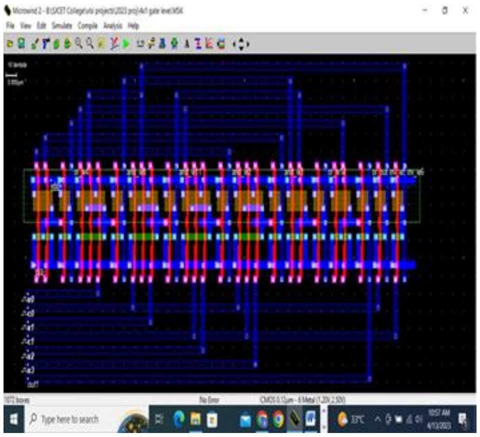


Fig: 9 . Layout Diagram of Gate Level 4:1 Mux

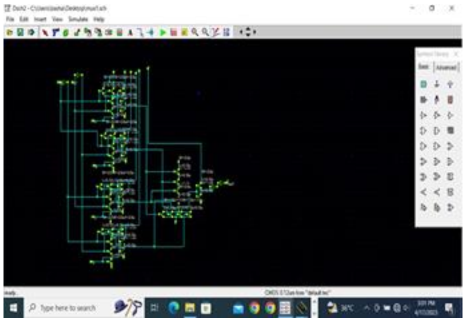


Fig: 10 . Schematic diagram of CMOS 4:1 Mux

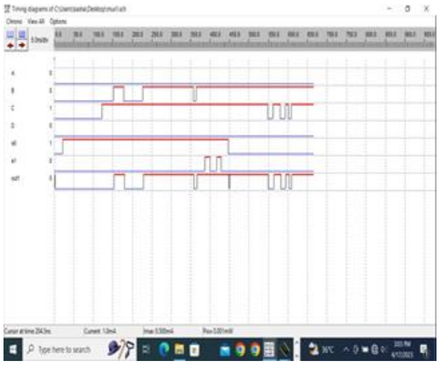


Fig: 11. Timing diagram of CMOS 4:1 Mux

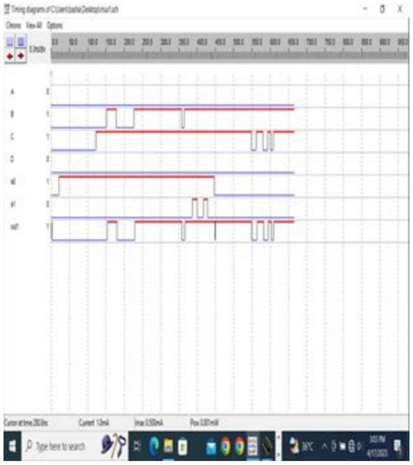


Fig: 12. Timing diagram of CMOS 4:1 Mux

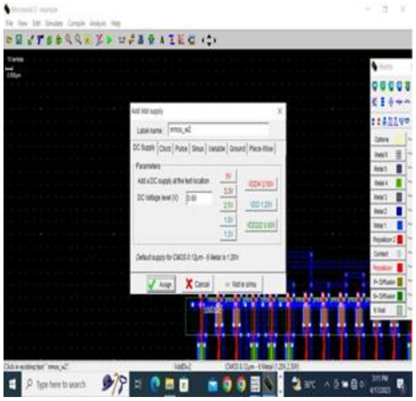


Fig: 13. Layout of 120nm with Vdd = 1.80v

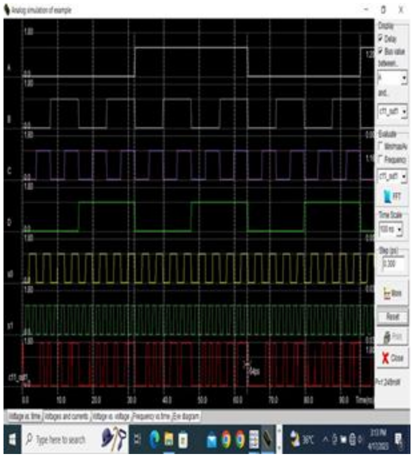


Fig: 14 . Simulation Diagram of 120nm with Vdd=1.80v

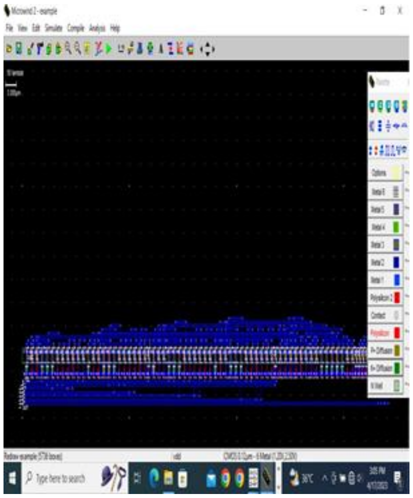


Fig: 15. Layout of 120nm with Vdd = 1.20v

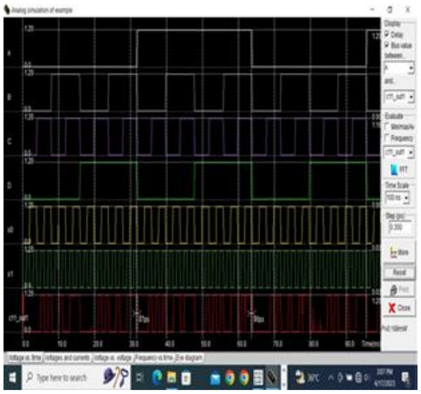


Fig: 16 . Simulation Diagram of 120nm with Vdd=1.20v

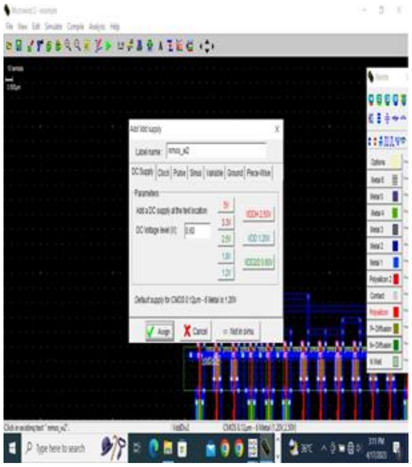


Fig: 17 . Layout of 120nm with Vdd = 0.60v

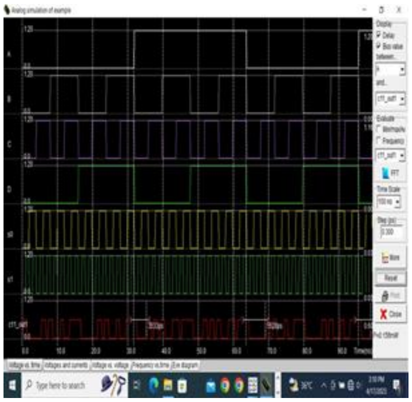


Fig: 18 . Simulation Diagram of 120nm with Vdd=0.60v

TABLE: 2 : Power Dissipation With CMOS Level for 120nm Technology

Technology	**Supply (Vdd)**	**Power dissipation**	**No. of Metals**
120nm	**1.80v**	**1.243mW**	**6**
	1.20v	**0.199mW**	**6**
	0.60v	**0.158mW**	**6**

IV.B. 80nm Layout Diagrams and Simulation:

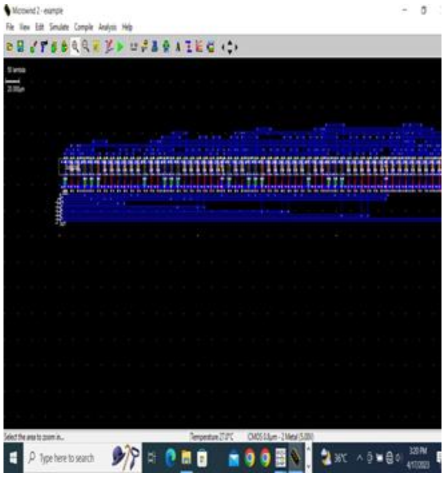


Fig:9.13. Layout of 80nm with Vdd = 5v

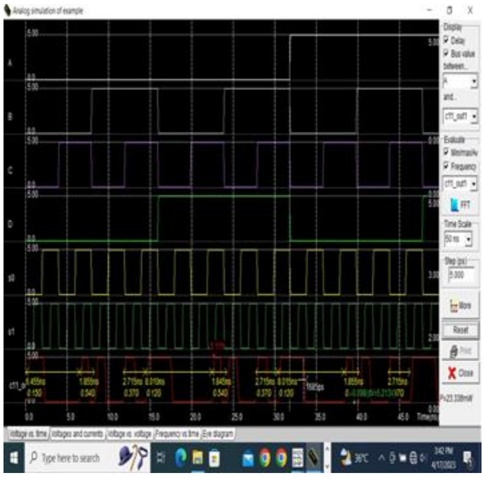


Fig:9.14. Simulation Diagram of 80nm with Vdd=5v

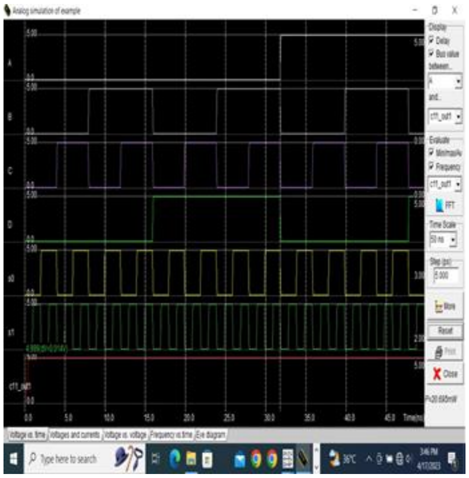


Fig:9.15. Simulation Diagram of 80nm with Vdd=3v

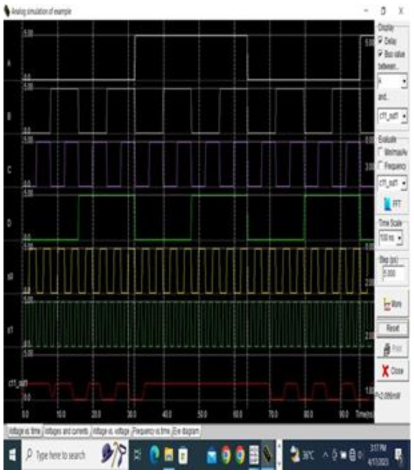


Fig:9.16. Simulation Diagram of 80nm with Vdd=1.80v

TABLE: 3 : Power Dissipation With CMOS Level for 80nm Technology

Technology	**Supply (Vdd)**	**Power dissipation**	**No. of Metals**
80nm	**5.0v**	**23.38mW**	**2**
	3.0v	**20.695mW**	**2**
	1.80v	**2.086mW**	**2**

V. CONCLUSION:-

In conclusion, the project on designing a low power 4:1 multiplexer using voltage scaling technique has been successful in achieving its objective of reducing power dissipation while maintaining high performance. By utilizing voltage scaling techniques such as reducing the supply voltage and using dynamic voltage scaling, the multiplexer was able to operate with lower power consumption without sacrificing its functionality.

The simulation results showed that the proposed design was able to reduce power consumption by up to 50% compared to traditional designs. Additionally, the multiplexer was able to maintain high performance in terms of delay and signal integrity.

The implementation of this low power 4:1 multiplexer can have significant benefits in various applications that require high-performance circuits with low power consumption, such as in portable devices, IoT, and biomedical applications. Overall, the project has demonstrated the potential of voltage scaling techniques in reducing power consumption and can serve as a basis for further research in this area".

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